REMARKS:

Applicant has carefully studied the nonfinal Examiner's Action and all references cited therein. The amendment appearing above and these explanatory remarks are believed to be fully responsive to the Action. Accordingly, this important patent application is now believed to be in condition for allowance.

Applicant responds to the outstanding Action by centered headings that correspond to the centered headings employed by the Office, to ensure full response on the merits to each finding of the Office.

Claim Objections

The Office has objected to claims 2-3 because they appear to be part of claim 1. Appropriate correction is submitted in this response by amendment to the claims.

Claim Rejections – 35 U.S.C. § 102

Applicant acknowledges the quotation of 35 U.S.C § 102(b).

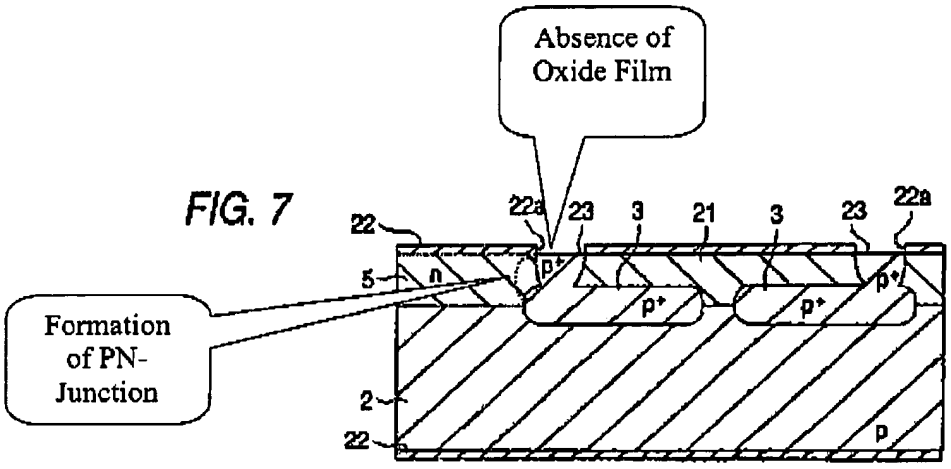
Claims 1-7, 9 and 11-12 stand rejected under 35 U.S.C § 102(b) as being clearly anticipated by Ishida et al. (U.S. Patent No. 5,830,777). Applicant respectfully submits that Ishida et al. does anticipate as the reference does not contain all the elements recited in the claims at bar.

With specific reference to Claim 1, the Office states that Ishida discloses a method comprising the steps of providing a silicon wafer 2, diffusing the wafer with dopant 23, whereby the diffusion creates a PN-junction throughout the surface of the wafer (Fig. 7), providing a mask 25, positioning the mask 35 in overlying relation to the surface of the wafer, etching the wafer to create recessed areas coincident with the patterned oxide (Fig. 10), the recessed areas characterized by the absence of surface PN-junction (since they are removed), hydrofluoric acid etching the wafer to form porous silicon 24 thereon, whereby the porous silicon is formed coincident with the surface area characterized by the absence of surface PN-junction, subjecting the wafer surface to wet etching resulting in dissolution of the porous silicon (Fig. 10).

Applicant respectfully submits that Ishida et al. does not anticipate because it does not describe the steps of etching the wafer to create recessed areas coincident with the patterned oxide, the recessed areas characterized by the absence of a surface PN-junction, and hydrofluoric acid etching the wafer to form porous silicon thereon, whereby the porous silicon is formed coincident with the surface area characterized by the absence of the surface PN-junction.

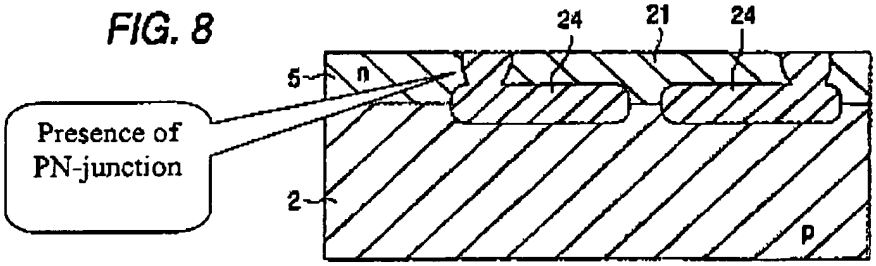
As shown with reference to Fig. 7 of Ishida et al., Ishida describes forming a n-type growth layer **5** on the upper surface of the silicon base plate **2**, then forming an oxide layer **22** on both sides of the silicon base plate **2**. After that, an approximately square opening **22a** is formed in a predetermined region on the oxide film **22** by means of photoetching. As such, the recessed area as described by Ishida is characterized by the absence of the oxide film, not by the absence of a surface PN-junction. Additionally, Ishida goes on to describe injecting boron into the opening **22a** by means of ion injection to form a second p-type layer **23** to communicate with the previously formed p-type diffusion layer **3**. By injecting the boron, Ishida describes creating a PN-junction between layer **23** and layer **5**, which is clearly not equivalent to an absence of a PN-junction as described by the present invention.

FIG. 7



As described by Ishida, the two p-type silicon layers **3** and **23** are then made porous to form porous silicon layer **24** as shown with reference to Fig. 8. As stated by Ishida at col. 6, line 32, only the p-type diffusion layers **3, 23** are selectively made to be porous. As such, Ishida does not describe forming porous silicon in a surface area characterized by the absence of a surface PN-junction as disclosed and claimed by the present invention. By contrast, Ishida describes forming porous silicon in the presence of (not the absence of) a PN-junction created by the boron injection and subsequent diffusion into the n-type layer **5**.

FIG. 8



As such, Applicant respectfully submits that Ishida et al. does not anticipate the present invention because it does not describe the steps of etching the wafer to create recessed areas coincident with the patterned oxide, the recessed areas characterized by the absence of a surface PN-junction, and hydrofluoric acid etching the wafer to form porous silicon thereon, whereby the porous silicon is formed coincident with the surface area characterized by the absence of the surface PN-junction.

For the reasons cited above, Applicant believes that amended independent claim 1 is not anticipated by Ishida and is believed to be in condition for allowance.

Claims 4-14 are dependent upon claim 1, and are therefore allowable as a matter of law.

If the Office is not fully persuaded as to the merits of Applicant's position, or if an Examiner's Amendment would place the pending claims in condition for allowance, a telephone call to the undersigned at (727) 507-8558 is requested.

Very respectfully,

SMITH & HOPEN

By:_____

Dated: January 24, 2006

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CERTIFICATE OF FACSIMILE TRANSMISSION
(37 C.F.R. 1.8(a))

I HEREBY CERTIFY that this Amendment A, including Amendments to the Claims, and Remarks is being transmitted by facsimile to the United States Patent and Trademark Office, Art Unit 1765, Attn.: Anita Karen Alanko, (571) 273-8300 on January 24, 2006.

Dated: January 24, 2006

Deborah Preza